CLAIMS

What is claimed is:

1. 1. A computer-implemented method comprising the steps of:

calculating by means of software a phase lock loop (PLL) voltage controlled oscillator (VCO) output signal frequency in response to a desired output clock frequency;

calculating by means of software a feedback divider ratio for said PLL in response to said VCO output signal frequency; and

generating by means of software a transistor level netlist for an analog PLL core, said analog PLL core having a VCO with said VCO output signal frequency and a feedback divider with said feedback divider ratio;

laying out a semiconductor chip, said semiconductor chip layout including said layout tile;

integrating said analog PLL core transistor level; netlist into a transistor level netlist of said semiconductor chip;

verifying said semiconductor chip layout by comparing connections described in said semiconductor chip layout against connections described in said semiconductor chip transistor level netlist;

checking said verified layout for compliance with design rules for a semiconductor chip manufacturing process; and

generating masks for said semiconductor chip after said verified semiconductor chip layout design rule check is completed.